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		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L10	L9 and l4	4
☐	L9	display near3 controller	54593
☐	L8	19990126	0
☐	L7	L5 and l2	6
☐	L6	L5 and l4	0
☐	L5	picture-in-picture	2580
☐	L4	19990126	19
☐	L3	L2 and (alteration)	38
☐	L2	(display or displaying) near8 (image or data) near8 (plurality adj2 (computer or device))	674
☐	L1	(display or displaying) near8 image near8 (plurality adj2 (computer or device)) near8 (display adj3 data) near8 (communication adj3 data)	0

END OF SEARCH HISTORY

Previous Doc Next Doc Go to Doc#
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L10: Entry 1 of 4 File: USPT Mar 20, 2001

DOCUMENT-IDENTIFIER: US 6204864 B1
TITLE: Apparatus and method having improved memory controller request handler

Abstract Text (1):
A computer system includes one or more display devices, such as a cathode ray tube (CRT) or liquid crystal display (LCD) for providing a visible display to a user of the computer system. The computer system includes a video display controller (VDC) with a graphics generator. This VDC receives image information, such as text or graphics generated by a processor (CPU) or retrieved by the CPU from another facility (such as a CD-ROM) of the computer system, and provides signals driving one or both of the CRT or LCD displays. The VDC includes a sequencer and controller (SEQC) for a dynamic random access memory (DRAM) which is interfaced with the VDC. The SEQC arbitrates requests from various devices of the computer system for access to the DRAM, and facilitates these access according to a multi-tiered priority scheme. Accordingly, more efficient access to the DRAM is insured for the various devices of the computer system, and utilization of the DRAM, as well as the time of devices which are sometimes required to wait for access to the DRAM is improved.

Application Filing Date (1):
19980717

Brief Summary Text (2):
The subject matter of the present application is related to subject matter disclosed in U.S. patent application Ser. No. 08/486,796, which was filed on Jun. 7, 1995, and has now issued as U.S. Pat. No. 5,694,141 for a Computer System with Double Simultaneous Displays Showing Differing Display Images; in U.S. patent application Ser. No. 08/485,876, which was filed on Jun. 7, 1995, and has now issued as U.S. Pat. No. 5,673,416 for a Display FIFO Module including a Mechanism for Issuing and Removing Requests for DRAM Access; in U.S. patent application Ser. No. 08/487,120 which was filed on Jun. 7, 1995, and has now issued as U.S. Pat. No. 5,724,063 for a Computer System with Dual-Panel LCD Color Display; and in U.S. patent application Ser. No. 08/487,121, which was abandoned in favor of U.S. patent application Ser. No. 08/872,244, which was filed on Jun. 10, 1997, for a Computer System with Video Display Controller having Power Saving Modes now U.S. Pat. No. 5,886,689.

Brief Summary Text (4):
The present invention relates generally to a computer system with one or more display devices, such as a cathode ray tube (CRT) or liquid crystal display (LCD) for example. The display devices provide a user of the computer system with a visible display of computer data, such as text or graphics. More particularly, the present invention is in the field of a computer system having a graphics generator, and a video display controller (VDC) for such a computer system. Via a bus interface, the VDC receives image information, such as text or graphics generated by a processor (CPU) or retrieved by the CPU from another facility (such as a CD-ROM) of the computer system, and provides signals driving one or both of the CRT or LCD displays.

Brief Summary Text (12):

Thus, page-mode access to the DRAM is much more efficient in terms of time utilization than is random access to the DRAM because of the many page breaks required for random access. When page-mode is not maintained for the DRAM, then at least one preparatory pre-charge cycle must be conducted to allow access to another different page of the DRAM in addition to the time interval required to write the data to or read the data from the memory cells. When access is allowed to the DRAM for the bit-BLT, these accesses will ordinarily be multi-page accesses which consume considerable time, but a request for this access does not require that immediate access to the DRAM be granted. On the other hand, CPU (local bus) access to the DRAM is usually a single-page access, requires considerably less time than a bit-BLT access, and also does not require that a request result in immediate access. However, when the CPU is required to wait for DRAM access, the system throughput is decreased and the WINMARKS (industry standard performance bench marks) for the computer system also are decreased. Further, the display FIFO of a graphics controller also requests DRAM access, and may be envisioned as a storage tank of water (data) draining at a uniform rate from the bottom, and only occasionally being refilled from the top. The display FIFO stores image information to be sent to the display devices (i.e., to the CRT or LCD, for example). The rate of drainage of the data from the display FIFO depends on the mode of display operation. If the display is being operated in a gray-scale mode which requires four bits per pixel, then the display FIFO will not drain very fast. On the other hand, if the user is operating the display in a color mode, then each pixel of the display may require eight bits, or sixteen bits, or possibly more than sixteen bits of information; and the display FIFO will drain correspondingly faster.

Brief Summary Text (13):
The display FIFO refills much faster than it drains. But refilling may be intermittent and interrupted for the allowance of other activities requiring access to the DRAM. Further, it must be understood that while the FIFO is being refilled, complete double-words of data must be input from the DRAM. If there is insufficient room at the top of the display FIFO to accept all of the last complete double-word of data being input at a particular time, then some of the existing data will be overwritten and lost. Conventionally, a FIFOLO request (a low priority request for DRAM access) is issued by the display FIFO to the DRAM controller as soon as the display FIFO has room at the top for at least one double-word of new data without overwriting existing data waiting to be sent to the display device.

Drawing Description Text (7):
FIG. 5 provides a schematic functional block diagram of the video display controller (VDC) of the computer system seen in the preceding figures;

Detailed Description Text (3):
FIG. 4 provides a schematic block diagram of the computer system 10, with the input devices all subsumed within one representative block 26. The input devices are interfaced with a microprocessor 28, which also has an interface with a memory facility 30. The memory facility 30 will include the floppy disk drive 20, and may include a hard disk drive, CD-ROM, and other devices. A data bus 32 interfaces with the microprocessor 28 and provides an interface with the output devices, including the LCD and CRT image display devices 14 and 24. The other output devices for the computer system 10 are subsumed in a representative block 34. In order to facilitate the interface with the image display devices 14 and 24, the computer system 10 includes a video display controller (VDC) 36 interfacing with the bus 32, and providing driving signals for the LCD 24 and CRT 14. The VDC has an interface with dynamic random access memory (DRAM), represented on FIG. 4 with the schematic blocks 38. Also, the VDC has an interface with a power management facility 40 of the computer system 10. A dedicated clock 42 provides a reference clock rate to the VDC 36.

Detailed Description Text (9):
Each of the hardware cursor generator 52, bit-BLT 54, and display FIFO 56 are also

interfaced with a DRAM controller 58. This DRAM controller 58, as will be further explained, implements the functions of the DRAM controller/sequencer described in general terms above to arbitrate and implement requests for access to the DRAM by various functional units of the computer system 10, including other portions of the VDC 36. As is seen in FIG. 5, the DRAM-controller 58 has an interface with the DRAM 38. For purposes of simplicity of illustration, the DRAM 38 is shown in FIG. 5 as a single functional block. However, those ordinarily skilled in the pertinent arts will recognize that this DRAM may comprise one or several DRAM chips. The display FIFO 56 has an interface (via the VGA controller 50 and DRAM controller 58) with both a palette controller 60, and with a liquid crystal display (LCD) interface controller 62. The palette controller implements the standard 256-by-18 VGA palette, while the LCD interface controller performs frame modulation and dithering for 64 shades of gray in monochrome mode operation; and 4K colors, with dithering for a full 256K colors in color mode operation.

Detailed Description Text (20):
Within SEQC 86 is a priority logic unit 90 implementing a logical selection process among the pending requests for access to the DRAM 38, as is illustrated in FIGS. 8 and 10. FIG. 8 represents the simpler alternative of a DRAM controller having only a single display FIFO 56, and will be considered first. Pending requests for access to the DRAM 38 are first of all assigned to one of two tiers (an upper tier and a lower tier), as will be further explained. Within the upper tier, pending requests are ranked in order of priority (numbered 1u through 5u). Similarly, within the lower tier, pending requests are ranked in order of priority (indicated as 1l through 3l). Within this logical structure of ranked pending requests for access to the DRAM 38, each upper-tier request may interrupt any existing access to the DRAM 38 granted in response to another upper-tier request with a lower rank, and may also interrupt an access granted in response to all lower-tier requests. Thus, if an access to the DRAM for the display FIFO is underway in response to a FIFOLO request (ranked 1l), and a request to refresh the DRAM is received by the SEQC (ranked 4u), then the display FIFO access is interrupted. The DRAM is then refreshed.

Detailed Description Text (25):
FIG. 10 graphically presents the priority logic scheme implemented by the priority logic unit 90 in the more complex alternative of a DRAM controller having two or more display FIFOs 56, 56', 56", etc. That drawing shows that the pending requests for access to the DRAM 38 are first of all assigned to one of three tiers (an upper tier, a middle tier, and a lower tier), as will be further explained. Within the upper tier, pending requests are ranked in order of priority (numbered 1u through 3u). It will be noted that this tier has several co-equal requests at one ranking level, as will be explained further. Within the middle tier, requests are ranked from 1m to 2m. Similarly, within the lower tier, pending requests are ranked in order of priority from 1l through 3l. Within this logical structure of ranked pending requests for access to the DRAM 38, each upper-tier request is placed in a queue of requests in that tier.

Detailed Description Text (32):
To appreciate this feature's advantage, consider the timing diagram of FIG. 14. For the sake of illustration, we assume a DRAM-access request from the mouse or some other device whose priority is higher than the displays'. The high level in FIG. 14's first row represents this request's initial presentation. The low-to-high transitions in other six rows indicate that all three displays present initially low-priority, and subsequently high-priority, DRAM-access requests while the mouse's request is still being serviced. Under such circumstances, the sequencer and controller accords none of the displays access until the mouse DRAM-access completion represented by the first row's high-to-low transition.

Detailed Description Text (37):
Of course it will be obvious to those of ordinary skill in the relevant art, after

study of the description set forth above in conjunction with the drawings, that principles, features and methods of operation of the described computer system with display and methods may be readily applied to other systems and devices, including but not limited to intelligent devices incorporating a display, embedded micro-controllers incorporating a user display, and intelligent input/output processing mechanisms including a display.

Detailed Description Text (38):
While the present invention has been depicted, described, and is defined by reference to particularly preferred embodiments of the invention, such reference does not imply a limitation on the invention, and no such limitation is to be inferred. The invention is capable of considerable modification, alteration, and equivalents in form and function, as will occur to those ordinarily skilled in the pertinent arts. The depicted and described preferred embodiments of the invention are exemplary only, and are not exhaustive of the scope of the invention. Consequently, the invention is intended to be limited only by the spirit and scope of the appended claims, giving full cognizance to equivalents in all respects.

CLAIMS:

1. A system comprising:

A) an input device for receiving inputs from a user of the system;

B) a central processing unit (CPU) interfacing with the input device and responding to the inputs by performing a processing function producing an output including display data;

C) a memory device interfacing with the CPU to provide memory storage of commands and data used by the CPU;

D) a plurality of output devices, each of which receives the output from the CPU and provides a sensible output response and includes a display device providing a visible image to the user in response to the display data;

E) a dynamic random access memory (DRAM); and

F) a video display controller (VDC) interfacing the DRAM to the CPU to forward display data thereto for temporary storage, the VDC including:

i) a plurality of display first-in-first-out (FIFO) memories, each display FIFO:

a) being associated with a different one of the display devices;

b) interfacing with the DRAM for receiving and temporarily holding display data to be imminently presented on the display device;

c) being of certain capacity and continuously providing the data to its associated display device while receiving data from the DRAM only intermittently; and

d) issuing a low-priority (FIFOLO) or high-priority (FIFOHI) request for access to the DRAM dependent respectively on whether a data level in the display FIFO is below a FIFOLO pointer or is below a FIFOHI pointer; and

ii) a sequencer and controller unit (SEQC) arbitrating access to the DRAM among the display FIFOs according to a multi-tiered priority in which the FIFOs' low-priority requests are ranked within a lower tier and the FIFOs' high-priority requests are ranked within a tier above the lower tier in an order opposite the order in which those FIFOs' low-priority requests are ranked in the lower tier, lower-tier requests not being enabled to interrupt any existing DRAM access, and requests in a

tier above the lower tier being enabled to interrupt an existing DRAM access granted by the SEQC in response to a lower-tier request.

9. For operating a system comprising an input device for receiving inputs from a user of the system; a central processing unit (CPU) interfacing with the input device and responding to the inputs by performing a processing function producing an output including display data; a memory device interfacing with the CPU to provide memory storage of commands and data used by the CPU; a plurality of output devices, each of which receives the output from the CPU and provides a sensible output response and includes a display device providing a visible image to the user in response to the display data; a dynamic random access memory (DRAM); and a video display controller (VDC) interfacing the DRAM to the CPU to forward display data thereto for temporary storage, a method comprising the steps of:

A) including in the VDC a plurality of display first-in-first-out (FIFO) memories, each display FIFO:

i) being associated with a different one of the display devices;

ii) interfacing with the DRAM for receiving and temporarily holding display data to be imminently presented on the display device;

iii) being of certain capacity and continuously providing the data to its associated display device while receiving data from the DRAM only intermittently; and

iv) issuing a low-priority (FIFOLO) or high-priority (FIFOHI) request for access to the DRAM dependent respectively on whether a data level in the display FIFO is below a FIFOLO pointer or is below a FIFOHI pointer; and

B) including in the VDC a sequencer and controller unit (SEQC); and

C) using the SEQC to arbitrate access to the DRAM among the display FIFOs according to a multi-tiered priority in which the FIFOs' low-priority requests are ranked within a lower tier and the FIFOs' high-priority requests are ranked within a tier above the lower tier in an order opposite the order in which those FIFOs' low-priority requests are ranked in the lower tier, lower-tier requests not being enabled to interrupt any existing DRAM access, and requests in a tier above the lower tier being enabled to interrupt an existing DRAM access granted by the SEQC in response to a lower-tier request.

17. A video display controller (VDC) that interfaces a dynamic access memory (DRAM) to a central processing unit (CPU) that provides display data to a plurality of display devices, the VDC comprising:

i) a plurality of display first-in-first-out (FIFO) memories, each display FIFO:

a) being associated with a different one of the display devices;

b) interfacing with the DRAM for receiving and temporarily holding display data to be imminently presented on the display device;

c) being of certain capacity and continuously providing the data to its associated display device while receiving data from the DRAM only intermittently; and

d) issuing a low-priority (FIFOLO) or high-priority (FIFOHI) request for access to the DRAM dependent respectively on whether a data level in the display FIFO is below a FIFOLO pointer or is below a FIFOHI pointer; and

ii) a sequencer and controller unit (SEQC) arbitrating access to the DRAM among the

display FIFOs according to a multi-tiered priority in which the FIFOs' low-priority requests are ranked within a lower tier and the FIFOs' high-priority requests are ranked within a tier above the lower tier in an order opposite the order in which those FIFOs' low-priority requests are ranked in the lower tier, lower-tier requests not being enabled to interrupt any existing DRAM access, and requests in a tier above the lower tier being enabled to interrupt an existing DRAM access granted by the SEQC in response to a lower-tier request.

Previous Doc Next Doc Go to Doc#

Previous Doc Next Doc Go to Doc#
First Hit Fwd Refs

Generate Collection

L10: Entry 3 of 4 File: USPT May 5, 1998

DOCUMENT-IDENTIFIER: US 5748189 A
**** See image for Certificate of Correction ****
TITLE: Method and apparatus for sharing input devices amongst plural independent graphic display devices

Application Filing Date (1):
19950919

Brief Summary Text (8):
It often is desirable to allow one air traffic controller to control the air space represented by a multiplicity of the display screens. In such a situation, it would be extremely inconvenient if the air traffic controller had to switch keyboards and mice every time he had to manipulate data on a different display screen/work station. Accordingly, systems are known in the prior art for allowing a single work station's keyboard and mouse set to control a plurality of display terminals. In such systems, a display controller card for each display terminal is plugged into a separate slot of a single work station. Specially designed binding software is run on that work station which binds all of the display cards together and allows the single keyboard and mouse associated with that work station to be used in connection with any of the display terminals associated with that work station.

Brief Summary Text (9):
A drawback of this type of system is that the various display terminals must be supportable by the binding software. In the real world, this generally means that the display terminals must be identical to each other or at least manufactured by the same vendor. Also, the binding software frequently will utilize extensions to the basic display language. For instance, air traffic control display software typically utilizes the X-Window language and protocol, which comprises 212 standardized commands. However, multiple screen control software commonly uses extensions to the basic language. Such software can be used only with displays and graphic controller cards which support those particular extensions. This severely limits the display terminal selection.

Brief Summary Text (22):
Some of the problems associated with the use of the multi-screen mode of X-Windows are illustrated in FIG. 3. In FIG. 3, screens 40 and 42 are of two different screen types (e.g., of different sizes and vendors). The host computer includes a graphic controller card 48 and 50 for each screen. Each graphic controller card is provided by the vendor of the display apparatus (screen) which it controls and is different from the other. The X-server includes distinct pieces of driver software 44 and 46 for driving each graphic controller card 48 and 50, respectively. Accordingly, the X-server software must be developed for the particular screen or screens which are to be driven by it. Thus, whenever a screen or graphic card controller is replaced or modified, the X-server software must also be replaced or modified.

Detailed Description Text (11):
An X-server is a piece of software which, among other things, receives commands and issues events in the X-Window protocol and language. It also converts commands and cursor movement data into a form understandable by the graphic controller cards for

causing a display apparatus to generate a particular display. Generally, and as used herein, X-protocol data transmitted by an application program are termed X-commands, while unsolicited X-protocol communications transmitted from an X-server to an application program are termed X-events. (Sometimes an application program requests data from an X-server: the response from the X-server is not considered an event, but a response to the query). The data received from input devices such as keyboards and mice (and from which an X-server may generate events for transmission to the application programs) is not X-protocol communication.

Detailed Description Text (12):
The present invention is meant to operate with commercially available display apparatus and graphic controller cards. Accordingly, the detailed operation and interfacing of graphic controller cards with their respective display apparatuses is not discussed herein.

Detailed Description Text (36):
In accordance with the present invention, each software block is separate and independent of the other software blocks. Accordingly, replacement of a display apparatus or graphic controller card does not require replacement of the X-server or peripheral manager software. Accordingly, multi-screen operation can be provided for different screens manufactured by different vendors having different sizes and/or resolutions without the need to have custom designed X-server or peripheral manager software for different screens.

Detailed Description Text (70):
Having thus described a few particular embodiments of the invention, various alterations, modifications and improvements will readily occur to those skilled in the art. For instance, it should be understood that, while the description above of some preferred embodiments of the invention utilize a mouse as the cursor control device, any number of other input devices, such as a trackball, pen mouse, light pen, or touch screen, would work equally as effectively with the present invention. Such alterations, modifications, and improvements as are made obvious by this disclosure are intended to be part of this description though not expressly stated herein, and are intended to be within the spirit and scope of the invention. Accordingly, the foregoing description is by way of example only, and not limiting. The invention is limited only as defined in the following claims and equivalents thereto.

CLAIMS:

6. A method of sharing an input device amongst a plurality of display devices in an apparatus comprising at least first and second display devices, a cursor control input device for issuing data for moving a first cursor on said first display device and a second cursor on a second display device, and at least a first X-server for receiving said data from said cursor control device and controlling said first display device, said method comprising the steps of;

(1) defining first and second mating transition windows on said first and second display devices, respectively,

(2) determining when said first cursor enters said first transition window,

when said cursor enters said first transition window,

(3a) grabbing from said X-server said data issued by said cursor control device,

(3b) positioning said second cursor in a position on said second display device, said position being a function of a position of said first cursor when it entered said first transition window,

(3c) masking said first cursor so that it does not appear on said first display device,

(3d) unmasking said second cursor so that it appears on said second display device, and

(3e) repositioning said first cursor on said first display device to a position spatially corresponding to said position of said second cursor on said second display device, and

(4) after said first cursor has entered said first transition window and until said second cursor enters said second transition window, simulating said data from said cursor control device to said second display device.

Previous Doc Next Doc Go to Doc#